Applicants note that the above-identified application, which was filed using numbered lines, was published on May 5, 2005 as United States Patent Application Publication No. 2005/0096755. In the amendment to the specification which follows, reference will be made to the pages and lines as in the application as filed, with a notation identifying the corresponding numbered paragraph in the application as published.

Please amend the specification as follows:

Please delete the paragraph starting at page 2, line 20 and continuing to page 2, line 17 (corresponding to paragraph [0003] of the specification as published) and replace with the following new paragraph:

--However, intensive work is also being conducted into standards for wireless networking of devices in the household. The so-called HIPERLAN Type 2 is cited as an example of a system which allows wireless networking of devices. In fact, this system has already been specified in an ETSI/BRAN standard. The exact title of this ETSI standard is Broadband Radio Access Networks (BRAN); High Performance Radio Local Area Network (HIPERLAN) Type 2. The complete standard comprises a number of parts, each of which can be ordered from ETSI in its latest version. Transmission of data as per this system takes place in the 5 GHz range. HIPERLAN2 devices contain a corresponding HIPERLAN2 interface which offers both send and receive functionality. The maximum speed of data transmission on a single channel is 32 megabits per second. This is achieved using a powerful Orthogonal Frequency Division Multiplexing (OFDM) transmission method. The following digital modulation methods can be used for the various subcarriers: BPSK, QPSK, 16QAM, and optionally 64QAM. With these digital modulation methods, it is vital when receiving that the signal amplitude at the demodulator input is set in a defined manner. Since the HIPERLAN2 interface is ~~essential~~ essentially constructed with two integrated circuits, one of which (the so-called front-end IC) is an analog IC, with the tuner and the mixer circuits, and the other of which (the baseband processor) is a digital IC, the actual signal amplitude is determined in the digital IC, but the receive gain has to be set in the analog IC. For this purpose, it must therefore be possible to

transmit data from the digital IC to the analog IC. Fluctuations in the gain setting as the result of applying setting values which transpire to be unreliable should also be avoided whenever possible. There is also a requirement for a simple bus connection between the digital IC and the analog IC, with as few wires or lines as possible. Since it is preferable for the gain setting to become effective without lengthy delays, data transmission must also be very fast.--

Please delete the paragraph at page 4, lines 8-38 (corresponding to paragraph [0012] of the specification as published) and replace it with the following new paragraph:

--Figure 1 shows the components of a HIPERLAN2 interface in a block diagram. The reference symbol 10 indicates the antenna or antenna system with a changeover switch between receive mode and send mode. The reference symbol 11 indicates the discrete components in which the RF signal is processed, including the send and receive filters and the balancing transformer between the antenna cable (coaxial cable) and the front-end IC 12. The front-end IC 12 is divided into an RF part 13 and a converter part 14 for generating the intermediate frequency. The dual conversion superheterodyne principle with conversion to a first and a second intermediate frequency is preferably implemented in the receive circuit, in order to reliably prevent image frequency reception. The send and receive paths have separate filter and amplifier stages. Two separate PLL synthesizer tuners are used for tuning on the send and receive paths. A further component of the front-end IC 12 is the serial bus interface for data transmission to and from the ~~baseband processor~~ central IC 15. The output amplifier for the send path is indicated in Figure 1 by the reference symbol 18, and is a discrete component to the front-end IC as outside. Said output amplifier can be set by the ~~baseband processor~~ central IC 15 via an analog line. Fine adjustment of the receive gain is however achieved by means of the additional send amplifiers in the RF section 13 of the front-end IC. The amplifiers for the receive path are provided in the front-end IC and are adjustable. The front-end IC 12 does not have a dedicated clock generator for transferring setting values to the relevant working registers. Therefore this clock is transmitted via the serial bus connection 19. --

Please delete the paragraph at page 5, lines 1-17 (corresponding to paragraph [0013] of the specification as published) and replace it with the following new paragraph:

-- The main component of the central IC 15 is a powerful processor, which uses software to implement the upper layers of the HIPERLAN2 protocol. In particular, this concerns the layers above the network layer (data link control layer). The same processor is also responsible for modulation and demodulation of the signals to be sent or received using the OFDM method. Another integrated component of the ~~peripheral~~ central IC 15 is the AD converter, which converts the intermediate frequency signal, that is output by the front-end IC 12, to a digital signal. The central IC 15 likewise contains a DA converter, which converts the digitally modulated signal to a corresponding analog signal. An external SDRAM memory module 16 is provided for storing data. The necessary software programs are stored in the flash memory 17, which is also external. Bus connections for an IEEE1394 bus interface or an Ethernet bus interface are also provided on the central IC 15. --

Please delete the paragraph at page 5, line 19 to page 6, line 8 (corresponding to paragraph [0014] of the specification as published) and replace it with the following new paragraph:

-- Figure 2 shows one part of the front-end IC 12, specifically the bus interface 20 and the status and setting registers that are connected to it. The bus interface 20 comprises a shift register 21 having a register width of 8 bits and a bus controller 22 which can be implemented using corresponding hardware as a status function. The bus driver 23 is also shown as a separate component and is activated for the send mode from the peripheral IC to the central IC. As previously mentioned, the bus connection itself comprises three lines. The data transmission line Data is directly connected to the input of the shift register 21. The output of the bus driver 23 is also connected to this data line. Conversely, the output of the shift register 21 is connected to the input of the bus driver 23. The control line of the bus connection is shown by the word Start in Figure 2. This line is connected to the bus controller 22. Since the front-end IC does not contain a dedicated clock generator, a clock line (CLK) is provided as a third line on the bus connection in order to prevent interference effects on the RF signal. This is connected to both the clock input of the shift register 21 and the bus controller 22. In addition to the status register 29 with a width

of 2 bits, the front-end IC includes a PLL1 register 27 with a width of 8 bits and a PLL2 register 28 with a width of 4 bits. The PLL1 register 27 is used to set the PLL, which stabilizes the frequency for converting the RF signal to the first intermediate frequency during the receive mode, or stabilizes the frequency for converting the intermediate frequency signal to the RF signal during these send mode.--

Please delete the paragraph at page 6, lines 20-24 (corresponding to paragraph [0016] in the specification as published) and replace it with the following new paragraph:

-- Both PLL registers 27 and 28 are read-only registers. The parallel outputs of the PLL registers 27 and 28 are hard wired to the corresponding programmable frequency dividers (not shown). The lock status for both PLLs is entered into the status register 29.--

Please delete the paragraph at page 6, line 32 to page 7, line 19 (corresponding to paragraph [0018] of the specification as published) and replace it with the following new paragraph:

-- In addition, an RXGain register 25 is provided for the receive mode. This is the working register for the receive gain setting. It also has a width of 8 bits. The parallel outputs of this RXGain register 25 are hard-wired to corresponding receive amplifiers in the RF path (not shown). According to the invention, a second register is also provided for the receive gain setting and functions as a preregister. This is shown as the RXGain Preload register 24 in Figure 2. It has a width of 8 bits, like the RXGain register 25. The parallel outputs of this ~~preregister~~ RXGain Preload register 24 are connected to the corresponding parallel inputs of the RXGain register 25. The parallel inputs of registers 24, 26, 27 and 28 are connected to the parallel outputs of the shift register 21. In this configuration, the PLL2 register 28 is connected only to the four most-significant bits of the shift register 21. The three least-significant bits of the shift register 21 are also connected separately to the bus controller 22. These three bits are used to transmit the register write address during data transmission from the central IC to the peripheral IC. The write operation to one of the write registers 24, 26, 27 and 28 will now be described in greater detail.

The address lines for the write registers 24, 25, 26, 27 and 28 are also shown in Figure. 2 and lead from the bus controller 22 to the relevant register. They also function at the same time as a write-enable signal, so that data waiting at the parallel inputs can be transferred to the register. --

Please delete the paragraph at page 7, line 30 to page 9, line 23 (corresponding to paragraph [0020] of the specification as published) and replace it with the following new paragraph:

-- The data transmission process for an operating parameter from the central IC 15 to the ~~peripheral~~ front-end IC 12 will now be described in greater detail, with reference to the signal diagram in Figure 3. The top line of Figure 3 shows the system clock with which the central IC 15 works. The clock frequency is 160 MHz. This is used to derive the clock CLK for data transmission between the peripheral and the central IC. The system clock is stepped down by a factor of 4 for this purpose, thereby giving a clock frequency of 40 MHz for the data transmission. The data transmission is started by the central IC 15 by sending a start pulse on the start line Start. As shown in Figure 3, the length of the start pulse corresponds to half the clock pulse period of the data transmission clock at 40 MHz. The rising edge of the start pulse resets the bus controller 22 if the High potential on the clock line is detected at the same time. Starting with the trailing edge of the bus clock following the rising edge of the start pulse, the register write address for the write operation is transmitted on the data line Data. The sampling instant for each bit is symbolized by a vertical dashed line. This vertical dashed line coincides with the rising edge of the bus clock (CLK) in each case. The clock cycles after the start pulse are counted in the bus controller 22. With the trailing edge of the third clock cycle after the start pulse, the register write address which is represented by the three least-significant bits of the shift register 21 is decoded internally in the bus controller 22, and a reservation flip-flop for the corresponding address line is set internally in the bus controller 22. Data transmission of the register write address is immediately followed by data transmission of the operating parameter. Eight bits are transmitted as an operating parameter in each case. Therefore a total of eleven bits are shifted into the shift register 21, of which only the last eight bits remain when the data transmission is complete. The first three bits, which relate to the register write address, have been

shifted out of the shift register 21 by this time and are therefore no longer available. With the trailing edge of the last clock cycle of the transmission of the eight data bits, the bus controller 22 generates a write pulse xxx_write. This write pulse is routed in parallel to all address lines except for the address line (rxg_valid) which leads to the ~~working~~ RXGain register 25. However, the write pulse is allowed through only on the address line which was previously selected by setting the reservation flip-flop when decoding the address. Consequently, the register write pulse reaches only the selected register, where it causes the data waiting at the parallel inputs of this register to be transferred into this register. If the selected register is the ~~preregister~~ RXGain Preload register 24, then the setting value in this register does not yet have any effect on the receive gain setting at this time. In this case, the value held in the ~~preregister~~ RXGain Preload register 24 is transferred to the ~~next~~ RXGain register 25 only following a further pulse on the start line. This transfer pulse does not differ from the aforementioned start pulse on the start line. However, it should be noted that it can be distinguished from the start pulse by virtue of the fact that at the instant this pulse is generated the clock line (CLK) is switched to Low, whereas the High potential is present on the clock line (CLK) in the case of a valid start pulse. It is therefore possible to generate a copy pulse on a further line (xxx_valid) by logically combining the clock line and the start line, where this copy pulse is routed only to the address line of the ~~working~~ RXGain register 25, and without previously setting a reservation flip-flop for this purpose. If security or safety considerations so require, the configuration can also be implemented in such a way that the copy pulse is allowed onto the address line of the working register only if the reservation flip-flop for the ~~preregister~~ RXGain Preload register 24 has been set previously. During the whole write cycle, the control line Output_Enable of the bus controller 22 is deactivated, i.e. is at Low potential. --

Please delete the paragraph at page 9, line 25 to page 10, line 12 (corresponding to paragraph [0021] in the specification as published) and replace it with the following new paragraph:

-- The operation for reading the status information in the peripheral IC 12 will now be described in greater detail, with reference to Figure 4. This data transmission is also initiated

from the central IC 15. The same designations are used for the lines in Figure 4 as in Figure 3. The central IC 15 again starts the data transmission with a start pulse on the start line. The status register read address is then transmitted to the ~~peripheral~~ front-end IC 12. The Output_Enable line of the bus driver 23 is activated by the trailing edge of the clock cycle in which the last address bit was transmitted. At the same time, the control line Load_Status is used to switch the multiplexers for the two most-significant bits of the status register 29, and the content of the status register 29 is copied into the two most-significant bits of the shift register 21 with the next rising edge of the bus clock. Since the bus driver is already switched on, transmission of the highest-order bit takes place via the bus line (Data) at the same time as this clock pulse. The next clock pulse triggers a shift operation in the shift register 21 and results in transmission of the second status bit. With the trailing edge of this clock cycle, data transmission to the central IC 15 is terminated because the control line Output_Enable is reset to Low and therefore the bus driver 23 is disconnected. During transmission of the status information, the internal control lines xxx_write and xxx_valid in the bus controller 22 are deactivated, i.e. set to Low. --